First Named Inventor	Giovanni Naso	COMMUNICATION REGARDING CERTIFICATE OF CORRECTION
Patent No.	6,947,323	
Issue Date	September 20, 2005	
Examiner Name	Tan T. Nguyen	
Attorney Docket No.	400.199US01	
Title: CHIP PROTECTION REGISTER UNLOCKING		

Attention Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant hereby requests issuance of a Certificate of Correction in U.S. Letters Patent No. 6,947,323 as specified on the attached Certificate (Form PTO/SB/44).

Applicant believes that some of the corrections are necessary due to Applicant errors of a clerical nature and therefore encloses the $100.00 Certificate of Correction Fee Under 1.20(a). If deemed necessary, the U.S. Patent Office is authorized to charge any additional fees found due to our Deposit Account No. 501373. Please contact the undersigned attorney if you have any questions.

Respectfully submitted,

Date: 4/24/07

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PTO/SB/44 (04-05)
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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,947,323

APPLICATION NO.: 10/698,752

ISSUE DATE : Sept. 20, 2005

INVENTOR(S) : Naso et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 9, Line 51, delete "segments 416 and one or more protection registers 428 and" and insert --segments 416 and one or more protection registers 418 and--

Column 10, Line 12, delete "registers 428 and the associated lock bits are included as part " and insert --registers 418 and the associated lock bits are included as part --

Column 10, Line 15, delete "128 and lock bits to be accessed for read and write" and insert --418 and lock bits to be accessed for read and write--

Column 10, Line 18, delete "register 428 is maintained as a writeable/eraseable memory" and insert --register 418 is maintained as a writeable/eraseable memory --

Column 10, Line 22, delete "428 and its current data contents." and insert --418 and its current data contents.--

Column 10, Line 26, delete "lock bits of the protection registers 428. The bond pad of the" and insert --lock bits of the protection registers 418. The bond pad of the--

Column 10, Line 29, delete "This allows the protection registers 428 to be" and insert --This allows the protection registers 418 to be--

Column 10, Line 32, delete "and erase circuit 432 allows the protection registers 428 and" and insert --and erase circuit 432 allows the protection registers 418 and--

Column 10, Line 37, delete "verification testing of the protection registers 428 and" and insert --verification testing of the protection registers 418 and--

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